Parasitic Challenges and Solutions Using Quantus QRC Extraction Solution for Advanced-Node FinFET Designs

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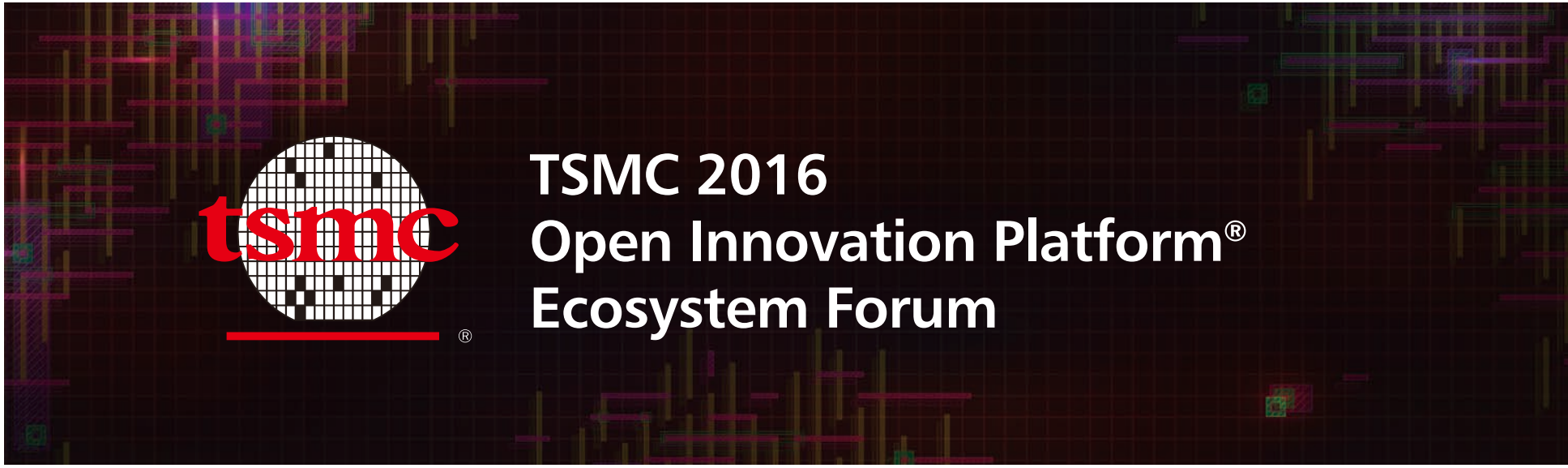


ABSTRACT

As process technology scaling reaches the realm of 10/7nmnm and below regimes, the challenges facing the foundry and design community are multi-faceted. The benefits of scaling have to be achieved with holistic process and design optimizations such that chip performance can still be improved per Moore's law, notwithstanding the physics effects, lithography effects (minus EUV) and other process effects at such atom level physical dimensions.

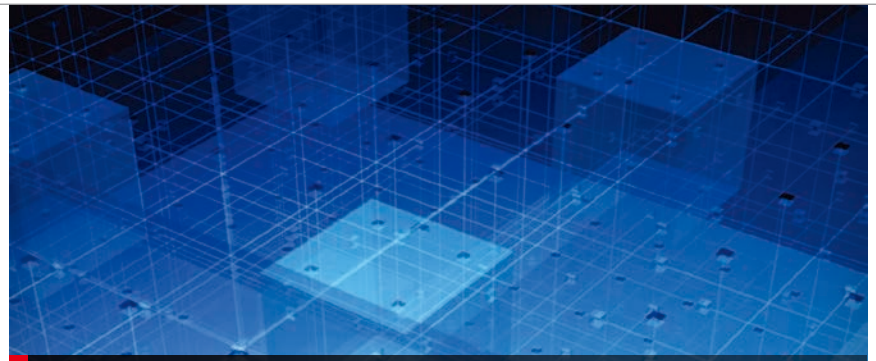
In this paper, the challenges of quasi-3D MEOL parasitic capacitance modeling, 10/7nmnm specific color mask modeling for lithography effects, as well as high performance blocking modeling are outlined and the subsequent validations and application of these modeling and extraction technologies for 10nm process development and designs are presented.

The most challenging aspect of MEOL parasitic modeling and model-based capacitance extraction is the introduction of 3D FinFET transistors which leads to severe 3D fringing cap distributions around MOS devices. In the 10/7nmnm 3D FinFET process node, the 3D MEOL modeling challenges are compounded by the unique 3D layouts which are necessary for process and design and optimizations. Quantus's unique quasi-3D modeling technology enabled the most silicon accurate extractions of FinFET-based designs such as standard cells, SRAM and PLL/VCO, which are the foundation of process development for 10/7nmnm process node.

For BEOL development, the impacts of HPB, with the intention of improving design performances, need to be accurately modeled by parasitic capacitance extractors such that large SOC designs with the aforementioned special process feature are possible. With EUV technology still absent from 10/7nm node, the needs for multiple patterning process steps mandate the development of new color aware mask modeling and extraction technologies in order to enable the shortest path of design to silicon.

SRAM design spans both MEOL and BEOL. It is a key part in the development of new process nodes in terms of process optimizations for best IP performance and lowest power consumptions. Consequently, It is essential that SRAM extractions have very tight capacitance accuracy, perfect bit-line match, as well as very good reduction accuracy, manageable simulation runtime for timing, EM/IR flow with large macros. Hence, there is a need for massively parallel field solver (3D) capability which is required to extract accurately without elongating extraction runtimes.

From designer's point of view, a tightly integrated extraction capabilities in implementation is a MUST at these FinFET nodes. In addition to the challenges presented for these nodes, we will also discuss the accuracy discuss the accuracy correlation with 3D field solver and performance of the extraction tool in addition to overall convergence and productivity benefits of the flow at 16nm and below nodes including 7nm.



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Hao Ji, R&D Group Director
Hitendra Divecha, Product Management Director
TSMC OIP Ecosystem Forum
San Jose, California
September 22, 2016

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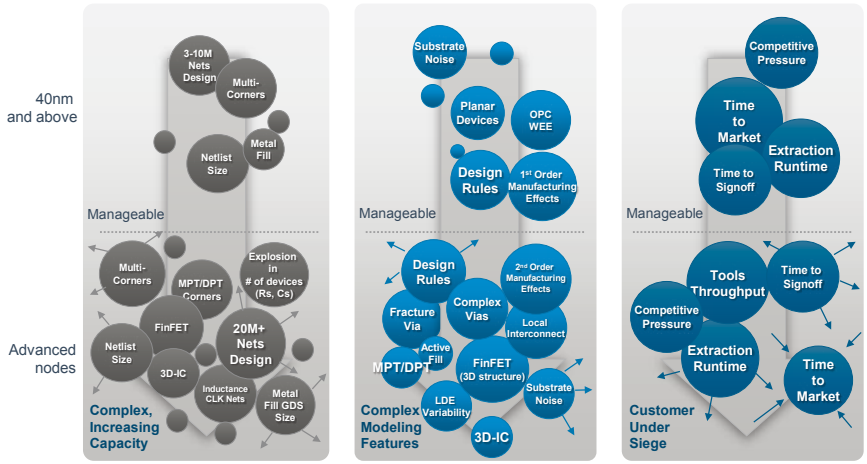
Evolving Requirements



Design complexity view | Modeling challenges view | Customer view

Signoff is becoming a bottleneck in design closure

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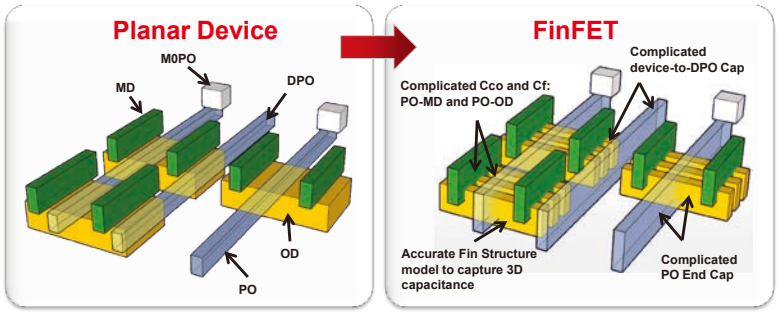
Enhance RC Modeling Capability to Enable Accurate Extraction

- More layers to be handled
  - Middle-end: New and expanded structure of middle-end
  - Front-end: Dedicated layers for SRAM instead of sharing with logic
  - Back-end: More metal schemes for customers to choose from
- More RC effects to be modeled



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7nm Parasitic Challenges

- FEOL: FinFET
- Dominated by fringe 3D capacitances in from gate, fins
- Thickness of gate introduces new capacitances components to fins (s/d)
- Cfi table for better FinFET device accuracy control

- MEOL: New M0 routing layer and local interconnect layer
- Explosions of R and hence better handling techniques are required to expedite post layout simulation
- More capacitances to M0/V0 (MEOL) contacts
- Tap via extension resistance modeling

- BEOL: Multiple patterning
- Different multi-color dependent color bias for logic and SRAM
- Required design methodology change
  - Best suited for repeated patterns such as memory designs, or track/grid based logic application
  - Pre-determined color due to color-dependent width bias
- Few changes in manufacturing effect table for erosion and viaR modeling
- Bridge via and pillar via

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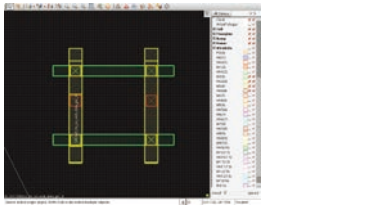
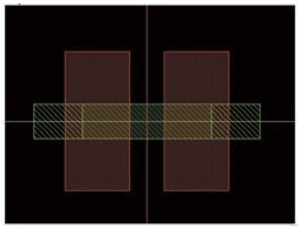
10/7nm Modeling Features

- Pillar vias
  - Required to minimize resistance (hence wire delay)
- Bridge vias
  - Required to provide flexibility in PG nets routing





Cadence® Quantus™ QRC Extraction Solution models these features accurately!

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Via Array, Bridge Via, Pillar Via Modeling

Via Array
- Number of metal landing pads – top and bottom are same
- Number of cuts >=1

Bridge Array
- Number of metal landing pads – top and bottom are different
- Number of cuts = 1
- TSMC N10 onwards

Pillar Via
- Number of metal landing pads – top and bottom are different
- Number of cuts >= max (top, bot) number of via landing pads
- TSMC N10 onwards

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Cadence + TSMC Delivers Signoff Extraction Solution to Mutual Customers

Engage
Collaborate on new modeling features requirements between Quantus R&D and TSMC including new DPT/MPT requirements for an extraction tool

Enable
Implement in Quantus and Quantus FS solutions, validate versus TSMC baseline, and enable PDK ready for mutual customers

Empower
Qualification and PDK delivery to foundry customers

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Key Challenges: PEX and Design Flow

1. Introduction of new and additional parameters e.g., Cgs, Res, and double and multiple patterning requires complex modeling to provide better accuracy
2. Explosion in parasitics results in bigger netlist impacting post-layout simulation performance
3. Lack of in-design extraction and signoff methodology and integration in implementation platforms impact convergence and loss of productivity
4. Signoff quality extraction is required during timing ECO optimization to reduce number of iterations to meet tape out schedule
5. Tightly integrated EMIR solution is a MUST to tackle complex EM rule checks required for FinFET designs

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Quantus QRC Extraction

Extraction you trust!

Accuracy
- Best accuracy vs foundry golden
- Color-solving extractor (DPT/MPT/SADP)
- Built-in 3D field solver, Quantus FS

Performance
- Massively parallel—100s of CPUs
- Fastest single and multi-corner extraction
- 2X smaller netlist for faster simulation runtimes

Productivity

Integrated with
- Innovus for digital extraction
- Virtuoso for transistor extraction
- Tempus, Voltus, Voltus-Fi, and PVS
- Automotive extraction
- Substrate Noise Analysis
- Inductance extraction for GDS and LEF/DEF

Market Leader

Quantus solution is industry's most trusted parasitic extraction tool that is used in production by leading foundries in advanced nodes 10nm and below!

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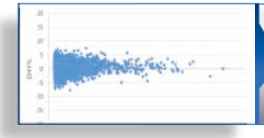
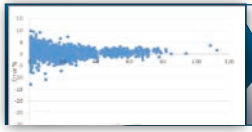
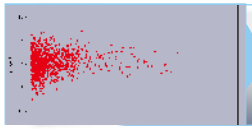
1 Best-in-Class Accuracy for First-Time Silicon Success—100% Pass Rate @ TSMC



7nm design
1502 all critical nets
Mean = 0.1%



7nm design
1324 < 7fF
Mean = 0.1%



7nm design
178 >= 7fF
Mean = 0.1%

Quantus solution vs Quantus FS for TCAP correlation for TSMC 7nm Certification

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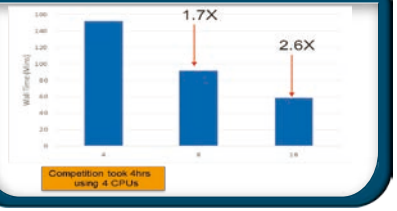
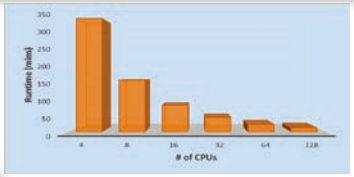
2 Fastest Extraction Tool in the Market for FinFET Designs

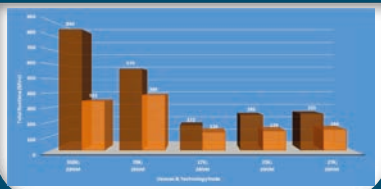
~2X Faster; 16nm SoC Design; 6 Corners



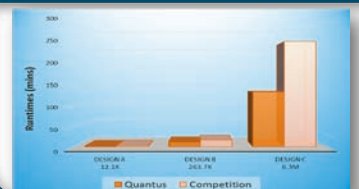
Linear Scalability for SoC Designs



Up to 2X Faster for Transistor Extraction



~2X Faster for 16FF+ SRAM Design



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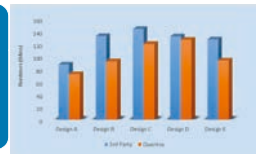
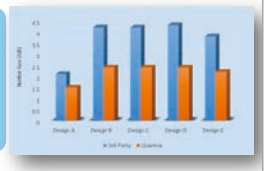
2 Smallest Netlist than Any Other Extraction Tool in the Market

10nm SRAM Designs

1 Extraction Runtime



2 Smallest Netlist (~2X)



3 Most Accurate RCs

	Quantus
Max Error	4.4%
Mismatch	0.3%
Timing	3.5% / 0.35ps
Max RC reduction error = 0.4%	

Path to Faster Simulation Runtimes

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3 Innovus + Quantus Signoff Extraction

INNOVUS

Floorplanning
GigaPlace
GigaOpt
CCOpt
NanoRoute

Single 'qrctechfile'

Quantus QRC Extraction

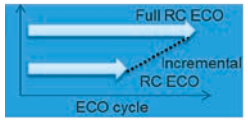
Quick Multi-Corner RC Analysis
3X faster Turbo Quantus early analysis

Accuracy

Incremental RC
3X Faster Signoff ECO with Integrated Quantus

Signoff Quantus

Performance

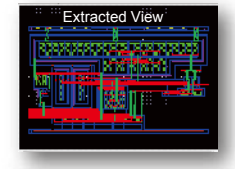


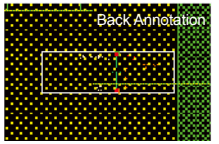
	Mean	STDev
TQuantus vs Quantus	1.47%	3.16%
IQuantus vs Quantus	-0.36%	1.19%

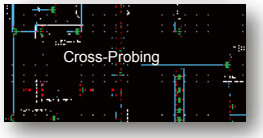
Innovus + Quantus—Only tightly-integrated solution in the industry

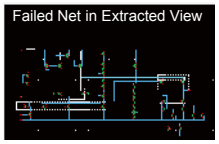
3 Virtuoso + Quantus Signoff Extraction

MODGEN Creation
Device Placement
Electrically Aware Net Routing
In-Design Verification
Extraction
LAYOUT









No stream in and out; executed from Virtuoso UI

Extracted view flow enables faster circuit debugging in Virtuoso ADE

Accurate cross-probing allows for faster timing verification in Virtuoso ADE

Single extracted view for 'N' number of process corners improving debugging efficiency

Supports hierarchical extraction

Fully supported in OA

Virtuoso + Quantus—Only tightly integrated solution in the industry

4 Quantus + Tempus ECO + Innovus Eliminates Tapeout Schedule Risk

Signoff runs under the hood from a single cockpit (no external files to transfer)

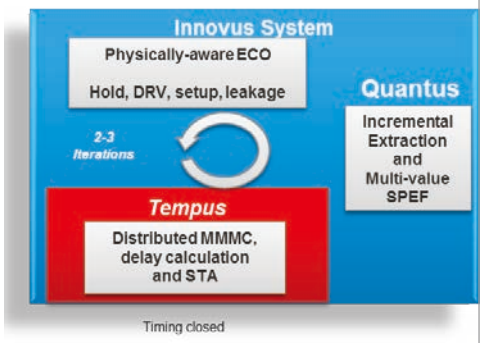
Unified engines with Innovus solution for both Quantus and Tempus solutions, strong correlation between post-P&R timing and ECO

Strong correlation between post-P&R extraction, timing, and ECO

Uses either IQuantus or Signoff Quantus

Multiple placement scenarios considered simultaneously, 100% legalized buffer placement

Tempus Physically Aware ECO



Tempus physically aware ECO results in 99% convergence per iteration

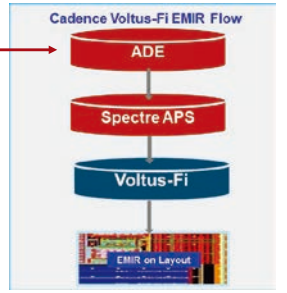
5 Quantus + Voltus-Fi for Accurate EMIR Analysis

Virtuoso Flow

MODGEN Creation
Device Placement
Electrically Aware Net Routing
In-Design Verification
Extraction
LAYOUT

xDSPF

Voltus-Fi



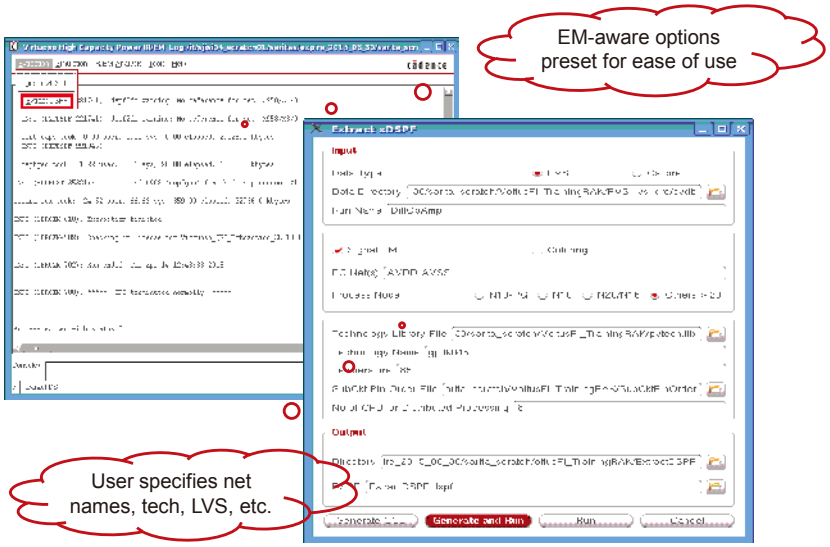
Comprehensive solution in an integrated Virtuoso flow for EMIR and PowerMos

Only Voltus-Fi solution works with Quantus solution for TSMC 16/10nm and below

Integrated—execute Quantus solution under the hood from Voltus-Fi solution

*Cadence Spectre® eXtensive Partitioning Simulator (XPS)

Voltus-Fi Embedded Quantus QRC Settings



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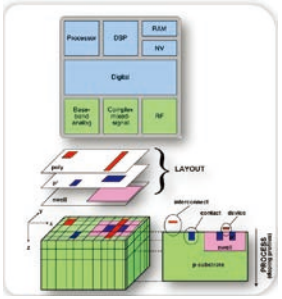
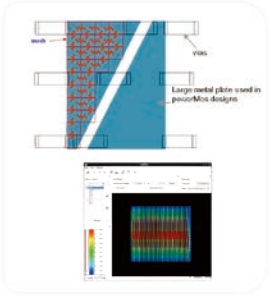
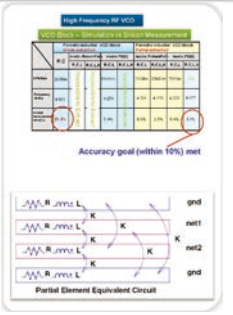
Market-Leading Features in Virtuoso Platform

Substrate Noise Analysis	PowerMos Extraction	Inductance Extraction
		
Noise analysis between analog block-block or digital to analog block	Support automotive designs; high-voltage/current, wide-metal designs	Supports partial element equivalent circuit (PEEC), high-frequency effects, and interconnect fracturing
Full 3D substrate model, accurate within ~7% of measurement data	High-accuracy Rdson	Silicon proven within 1.1% of measurement and Fast Henry
Provide isolation strategies (guardrings) to reduce noise in design	Integrated flow in Virtuoso platform with Voltus-Fi solution and Spectre XPS	Supports frequency points from DC to ~100GHz with a single extraction run

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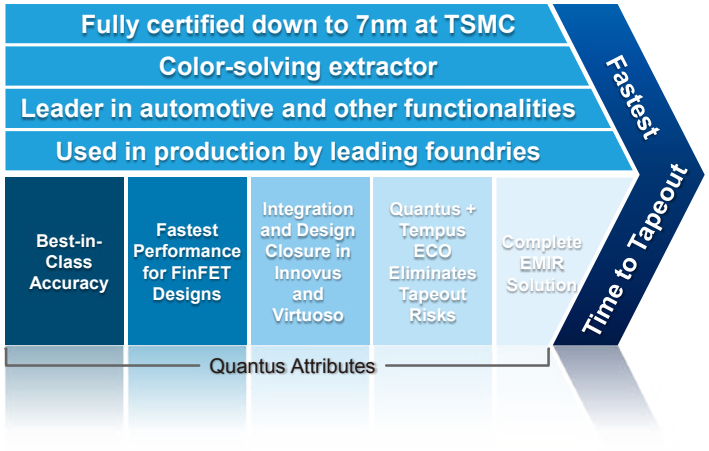
Summary



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